REMARKS

Claims 5-13, and 17 are pending in this application. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Allowable Claims

Applicants gratefully acknowledge that claims 6-13 are merely objected to as depending from a rejected base claim, but are otherwise allowable.

Rejections under 35 USC §102(b)

Claim 5 is rejected under 35 USC §102(b) as being anticipated by Edwards et al (U.S. Patent No. 5,625,568).

Applicants respectfully traverse this rejection.

Claim 5 has been amended to recite "modifying layout pattern data of said embedded array by detecting and removing a portion of an impurity region in a basic cell based on layout data of contact holes."

Edwards et al discloses a design system for compacting the integrated circuit layout with standard cell components. As indicated in the claims of Edwards et al, the circuit layout database stores a connectivity data structure representing the integrated circuit layout as a set of cells. A cell is defined as a given material or as empty, and the data structure includes data representing points defining edges and boundaries of said cells.

In Edwards et al, the data structure further includes connector cell data fields to identify whether each cell forms a portion of a connected group of cells. Accordingly, the integrated circuit layout is made into a compacted integrated circuit layout. The compacted integrated circuit layout is further re-organized. Thus, Edwards et al does not teach or suggest, among other things, "modifying layout pattern data of said embedded array by detecting and removing a portion of an impurity region in a basic cell based on layout data of contact holes," as recited in claim 5.

For at least these reasons, claim 5 patentably distinguishes over Edwards et al.

In items 4 and 5 of the Office Action, claim 5 is rejected under 35 USC §102(b) as being anticipated by Matsumoto (U.S. Patent No. 5,610,831).

Applicants respectfully traverse this rejection.

Matsumoto describes as follows:

> **The converted mask layout of FIG. 7B is formed by the process migration according to the original mask layout of FIG. 7A. The substrate contact 4 is selectively removed from the converted mask layout.** Accordingly, a space between transistors 1a and 8a on the converted mask layout is narrower than a space between the corresponding transistors 1 and 8 on the original mask layout. The design rule of the converted mask layout allows no substrate contact to be formed between the transistors 1a and 8a.
>
> Converting the original mask layout into the converted mask layout will be explained.
>
> **Substrate contacts are selectively removed from the original mask layout, to form a symbolic layout.** The substrate contacts are selectively removed according to a first design rule. Symbols on the symbolic layout are scaled according to the second prior art. The symbolic layout is then compacted with a symbolic compactor according to a second design rule whose minimum spacing is smaller than that of the first design rule. Substrate contacts are formed in a free space on the compacted layout, to form the converted mask layout.

Thus, Matsumoto removes a **substrate contact**. Matsumoto does not teach or suggest, among other things, "modifying layout pattern data of said embedded array by detecting and removing a portion of an impurity region in a basic cell based on layout data of contact holes.".

For at least these reasons, claim 5 patentably distinguishes over Matsumoto.

Thus, the 35 USC §102(b) rejections should be withdrawn.

It is submitted that nothing in the cited references, taken either alone or in combination, teaches or suggests all the features recited in each claim of the present invention. Thus all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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